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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/640,519	08/17/2000	Hiroaki Nakaoka	0819-408	6287

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EXAMINER
VU, DAVID

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/640,519	NAKAOKA ET AL.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

1. The Final Rejection base on Hsu et al (US 5,707,889) is withdrawn by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-7 and 9-10 are rejected under 35 U.S.C. 103(a) as being anticipated by Gardner et al (US 6,144,071) in view of Taniguchi et al. (US 6,211,003) and further in view of Chang et al. (US 5,817,562).

Regarding claims 1 and 9, Gardner et al, in related text and figure (Figure.4) disclose a method of fabricating a semiconductor device, the method comprising the steps of: forming a silicon oxynitride film22 on a substrate20; (Col. 8, Line 64 – Col. 9, Line. 4), after that, forming a semiconductor film 23 containing an impurity (Col. 10, Lines. 23-37) on the silicon oxynitride film 22 by patterning the polysilicon layer 23 (Col. 9, Lines. 5-9), and then forming a gate insulating film composed of SiON film22 by patterning the SiON film 22 (Fig. 13).

Gardner et al., disclose all claimed subject matter, but omits to introduce at least nitrogen into the silicon oxynitride film. Taniguchi et al., in related text (Col. 19, Lines. 15-33) disclose

performing a heat treatment, while keeping a surface of the silicon oxynitride film in contact with a gas containing nitrogen, to introduce at least nitrogen into the silicon oxynitride film. It would have been obvious to one of ordinary skill in the art at the time the invention was made to introduce nitrogen into the silicon oxynitride film since the interface state in the gate in the SiON film can be suppressed, and the electron trap in the SiON film can also be reduced, so that the hot carrier resistance in the SiON film can be improve. By nitrating the SiON layer, leakage current can be reduced.

Gardner et al. and Taniguchi et al., disclose all claimed subject matter, but omits the step of forming the polysilicon film containing an impurity before patterning the polysilicon film. Chang et al, in related text (Col. 1, Lines. 45-65) disclose the step of patterning the polysilicon film which is containing the impurity to form a gate electrode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a gate electrode by the method of Chang et al. to minimize electrical shorts and for greater product reliability.

In re claim 4, Taniguchi et al., disclose all claimed subject matter, but lacks to mention the temperature range for the heat treatment.Taniguchi et al., in related text disclose the heat treatment is performed at a high temperature (Col. 19, Lines. 25-29). Furthermore, the temperature is considered to involve routine optimization which has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the heat treatment temperature, etc. would have been obvious: "Normally, it is to be expected that a change in energy, concentration, thickness, dosage, temperature, or combination of any of them would be an unpatentable modification. Under some circumstances, however, changes such as these may impart

patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree ftom the results of the prior art such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 VSPQ 3 08 (CCPA 1945); In re Swenson 56 USPQ 3 72 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934). Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any temperature range suitable to the method in process of Hsu et al., in order to reduce the stress at the substrate-silicon oxynitride layer.

In re claims 5-7, Taniguchi et al disclose the step of subjecting the SiON in a gas atmosphere of NH_3 or NO_2 to introduce nitrogen into the SiON film.(Col. 19, Lines. 25-32)

In re claim 10, Gardner et al., in related text and figure (Fig. 20) disclose the first side wall with a L-shape45 cross section view is formed on the sides of the gate electrode 23 and a second side wall 46 that spreads over the side and base of the first side wall. (Col. 11, Lines. 53-67). The L-shape space is formed to prevent outdiffusion of impurities from substrate and to assist in prevention of bridging in the event of silicide formation.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the preceding rejection as applied to claim1 above, in further view of Sung (US 6,040,216).

Garner et al., disclose all claimed subject matter, but omits the forming of silicon oxynitride from N_2O gas.

Sung, in related text discloses the silicon oxynitride film is formed by using an N_2O gas (Col.4, Lines. 42-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a silicon oxynitride film by using N_2O gas because the nitrogen gas converts into a nitrogen ion, which is accelerated into the surface of the substrate.

4. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the preceding rejection as applied to claim1 above, in further view of Rodder (US 6,246,091).

Garner et al., disclose all claimed subject matter, but omits the forming of an amorphous silicon film on SiON layer. Rodder, in related text (Col. 5, Lines. 9-24) discloses forming, as the semiconductor film, an amorphous silicon film 126 on the gate insulating film122; implanting impurity ions into the amorphous silicon film; performing a heat treatment for activating the impurity to change the amorphous film126 into a polysilicon film126 then patterned and etched to form gate electrode 112 containing boron. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a gate electrode by the method of Rodder since boron could diffuse readily through amorphous silicon, it segregates into and through the gate insulator between the gate and the channel in a MOS type transistor. Boron does not move as readily in repaired or annealed silicon.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (703) 305-0391. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms., can be reached on (703) 308-4910.

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